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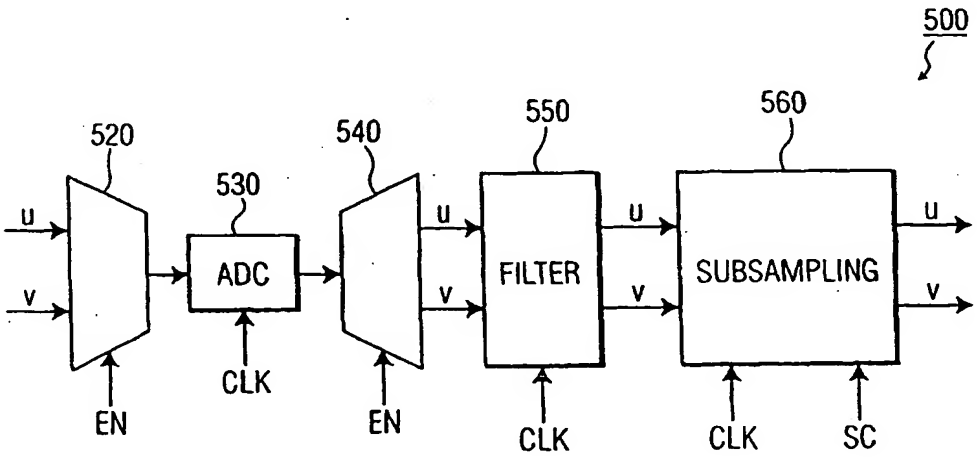

(57) Abstract: A system (400) such as an audio and/or video system includes a multiplexed analog-to-digital converter ("ADC") arrangement (500). The arrangement (500) includes an ADC (530) for converting first and second analog signals to first and second digital signals, respectively, and for outputting the first digital signal during a first time interval and outputting the second digital signal during a second time interval. A digital filter (550) is provided for filtering the first and second digital signals to generate first and second filtered signals, respectively, and for outputting the first and second filtered signals in a time-aligned manner during a third time interval.

WO 03/055207 A1

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MULTIPLEXED ANALOG-TO-DIGITAL CONVERTER ARRANGEMENT

The present invention generally relates to signal processing in systems such as video and/or audio systems, and more particularly, to an arrangement for time sharing an analog-to-digital converter ("ADC") in such systems that provides, among other things, time-alignment among output signals.

Time sharing an ADC for multiple input signals is a well-known way to reduce the number of ADCs in a system, such as a video and/or audio system. One technique for sharing an ADC in such systems involves simple multiplexing. FIG. 1, for example, illustrates a multiplexed ADC arrangement 100 employing simple multiplexing. In FIG. 1, a multiplexer 120 simultaneously receives analog U and V input signals, and is switched in dependence upon an enable ("EN") signal to output selected ones of the received analog U and V signals in an alternating manner. An ADC 130 receives the analog U and V output signals from multiplexer 120, and digitizes the received U and V signals in dependence upon a clock ("CLK") signal, wherein each interval of the CLK signal defines a single clock cycle or time interval. In FIG. 1, the frequency of the CLK signal may, for example, be two times the frequency of the EN signal. A demultiplexer 140 receives the digital U and V signals output from ADC 130, and is switched in dependence upon the EN signal to output the digital U and V signals. Table 1 below illustrates an exemplary operation of multiplexed ADC arrangement 100.

Clock Cycle	1	2	3	4	5
Analog U	45	46	47	48	49
Analog V	75	76	77	78	79
Mux Position	U	V	U	V	U
ADC Output	45	76	47	78	49
Demuxed U	45	45	47	47	49
Demuxed V	--	76	76	78	78

Table 1

As indicated in Table 1, the U and V output signals from demultiplexer 140 (i.e., Demuxed U / Demuxed V) are not time-aligned relative to the corresponding input signals to multiplexer 120 (i.e., Analog U / Analog V), but rather are staggered

in time. In other words, there is no clock cycle where the U and V output signals from demultiplexer 140 are time-aligned relative to the corresponding input signals to multiplexer 120. Note that for purposes of example and explanation, Table 1 depicts no signal delay through ADC 130 and demultiplexer 140. Also note in Table 1 that demultiplexer 140 produces both a U output signal and a V output signal during each clock cycle. One of these U and V output signals is a signal provided from ADC 130 during the current clock cycle, while the other of these U and V signals was provided from ADC 130 during a previous clock cycle.

For many applications, the lack of time-alignment between output signals, as represented in Table 1, poses no problem. In some systems, however, such time-alignment is necessary. For example, certain digital video systems having an integrated circuit ("IC") for providing a picture-in-picture ("PIP") function may require time-alignment between output signals.

One technique for providing time-alignment between output signals involves placing an analog sample-and-hold circuit in the signal path prior to the multiplexer that provides inputs to the ADC. FIG. 2, for example, illustrates a multiplexed ADC arrangement 200 employing a sample-and-hold circuit. In FIG. 2, a sample-and-hold circuit 210 receives and holds analog U and V signals until the next EN signal. A multiplexer 220 simultaneously receives the held analog U and V signals from sample-and-hold circuit 210, and is switched in dependence upon the EN signal to output selected ones of the received analog U and V signals in an alternating manner. An ADC 230 receives the analog U and V output signals from multiplexer 220, and digitizes the received U and V signals in dependence upon the CLK signal, wherein each interval of the CLK signal defines a single clock cycle or time interval. In FIG. 2, the frequency of the CLK signal may, for example, be two times the frequency of the EN signal. A demultiplexer 240 receives the digital U and V signals output from ADC 230, and is switched in dependence upon the EN signal to output the digital U and V signals. Table 2 below illustrates an exemplary operation of multiplexed ADC arrangement 200.

Clock Cycle	1	2	3	4	5
Analog U	45	46	47	48	49
Analog V	75	76	77	78	79
S&H U	45	45	47	47	49
S&H V	75	75	77	77	79
Mux Position	U	V	U	V	U
ADC Output	45	75	47	77	49
Demuxed U	45	45	47	47	49
Demuxed V	--	75	75	77	77

Table 2

As indicated in Table 2, the output signals from demultiplexer 240 (i.e., Demuxed U / Demuxed V) are time-aligned on every other clock cycle. For example, in Table 2 the output signals from demultiplexer 240 are time-aligned during clock cycle 2 and clock cycle 4. Note that for purposes of example and explanation, Table 2 depicts no signal delay through ADC 230 and demultiplexer 240. Also note in Table 2 that demultiplexer 240 produces both a U output signal and a V output signal during each clock cycle. One of these U and V output signals is a signal provided from ADC 230 during the current clock cycle, while the other of these U and V signals was provided from ADC 230 during a previous clock cycle.

Although the multiplexed ADC arrangement 200 of FIG. 2 provides some degree of time-alignment, it is problematic in that sample-and-hold circuits are not available in most standard cell libraries used to rapidly design an IC. As a result, the sample-and-hold circuit is considered a "custom" analog block that must be designed for the particular IC being developed. Custom analog blocks generally require additional development time, expense and risk in IC development.

Another approach for providing time-alignment involves placing an analog delay network prior to the multiplexed ADC. FIG. 3, for example, illustrates a multiplexed ADC arrangement 300 employing an analog delay network. In FIG. 3, an analog delay network 310 receives analog U and V signals and outputs the same with one of the U and V signals being differentially delayed with respect to the other signal (e.g., for one clock cycle). A multiplexer 320 receives the analog U and V

signals from analog delay network 310 (i.e. with one of the U and V signals having been delayed), and is switched in dependence upon the EN signal to output selected ones of the received analog U and V signals in an alternating manner. An ADC 330 receives the analog U and V output signals from multiplexer 320, and digitizes the received U and V signals in dependence upon the CLK signal, wherein each interval of the CLK signal defines a single clock cycle or time interval. In FIG. 3, the frequency of the CLK signal may, for example, be two times the frequency of the EN signal. A demultiplexer 340 receives the digital U and V signals output from ADC 330, and is switched in dependence upon the EN signal to output the digital U and V signals. Table 3 below illustrates the operation of multiplexed ADC arrangement 300.

Clock Cycle	1	2	3	4	5
Analog U	45	46	47	48	49
Analog V	75	76	77	78	79
Delay Network U	45	46	47	48	49
Delay Network V	--	75	76	77	78
Mux Position	U	V	U	V	U
ADC Output	45	75	47	77	49
Demuxed U	45	45	47	47	49
Demuxed V	--	75	75	77	77

Table 3

As indicated in Table 3, the output signals from demultiplexer 340 (i.e., Demuxed U / Demuxed V) are identical to the output signals produced from demultiplexer 240 in FIG. 2. That is, the output signals from demultiplexer 340 are time-aligned on every other clock cycle. For example, in Table 3 the output signals from demultiplexer 340 are time-aligned during clock cycle 2 and clock cycle 4. Note that for purposes of example and explanation, Table 3 depicts no signal delay through ADC 330 and demultiplexer 340. Also note in Table 3 that demultiplexer 340 produces both a U output signal and a V output signal during each clock cycle. One of these U and V output signals is a signal provided from ADC 330 during the current

clock cycle, while the other of these U and V signals was provided from ADC 330 during a previous clock cycle.

Although multiplexed ADC arrangement 300 of FIG. 3 also provides some degree of time-alignment, it is problematic in that the difference in magnitude and group delay characteristics between the two input paths can introduce undesirable differential frequency response effects. This problem is made worse by variations due to component tolerances.

Accordingly, there is a need for a multiplexed ADC arrangement that avoids the aforementioned problems, and provides time-aligned (i.e., co-located) output signals. The present invention addresses these and other issues.

In accordance with the present invention, a system such as an audio and/or video system includes a multiplexed ADC arrangement. The arrangement includes an ADC for converting first and second analog signals to first and second digital signals, respectively, and for outputting the first digital signal during a first time interval and outputting the second digital signal during a second time interval. A digital filter is provided for filtering the first and second digital signals to generate first and second filtered signals, respectively, and for outputting the first and second filtered signals in a time-aligned manner during a third time interval.

The above-mentioned and other features and advantages of this invention, and the manner of attaining them, will become more apparent and the invention will be better understood by reference to the following description of embodiments of the invention taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a diagram of a multiplexed ADC arrangement employing a simple multiplexing technique;

FIG. 2 is a diagram of a multiplexed ADC arrangement employing a sample-and-hold circuit;

FIG. 3 is a diagram of a multiplexed ADC arrangement employing an analog delay filter;

FIG. 4 is a diagram of an exemplary system including a multiplexed ADC arrangement according to principles of the present invention;

FIG. 5 is a diagram providing further details of the multiplexed ADC arrangement of FIG. 4; and

FIG. 6 is a flowchart summarizing exemplary steps for carrying out the present invention.

The exemplifications set out herein illustrate preferred embodiments of the invention, and such exemplifications are not to be construed as limiting the scope of the invention in any manner.

Referring now to FIG. 4, a diagram of an exemplary system 400 including a multiplexed ADC arrangement 500 according to principles of the present invention is shown. System 400 of FIG. 4 may be embodied as an audio and/or video system, such as a television signal receiver, a set-top box, video cassette recorder ("VCR"), digital versatile disk ("DVD") player, video game box, personal video recorder ("PVR") or other video and/or audio system.

In FIG. 4, system 400 includes multiplexed ADC arrangement 500 which enables its ADC (not expressly shown in FIG. 4) to be time-shared between input signals, U and V, and further enables such signals to be time-aligned when output. The U and V input signals may represent, for example, color difference signals in a digital video system, such as a high-definition television ("HDTV") system or the like. Multiplexed ADC arrangement 500 may, for example, be embodied on an IC. Although not expressly shown in FIG. 4, system 400 may also include other components, such as other ICs and other electrical and non-electrical components.

Referring now to FIG. 5, a diagram providing further details of multiplexed ADC arrangement 500 of FIG. 4 is shown. As shown in FIG. 5, multiplexed ADC arrangement 500 comprises a multiplexer 520, an ADC 530, a demultiplexer 540, a filter 550, and a subsampling device 560. As will be explained hereinafter, multiplexed ADC arrangement 500 provides time-aligned output signals without using an analog delay device prior to ADC 530.

In operation, multiplexer 520 simultaneously receives analog U and V input signals, and is switched in dependence upon the EN signal to output selected ones of the received analog U and V signals in an alternating manner. ADC 530 receives the analog U and V output signals from multiplexer 520, and digitizes the received U and V signals in dependence upon the CLK signal, wherein each interval of the CLK signal defines a single clock cycle or time interval. The EN and CLK signals may be generated by a clock generator or other device (not shown). According to an exemplary embodiment, the frequency of the CLK signal in FIG. 5 is two times the

frequency of the EN signal. For example, the CLK signal may exhibit a frequency of 18 MHz, while the EN signal may exhibit a frequency of 9 MHz. Accordingly, ADC 530 receives and digitizes only every other U and V signal input to multiplexer 520. That is, multiplexer 520 is switched such that every other U and V signal input to multiplexer 520 is lost. In this manner, ADC 530 outputs a digitized U signal during one clock cycle, and outputs a digitized V signal during the next clock cycle. Further details regarding this operation will be provided later herein.

Demultiplexer 540 receives the digital U and V signals output from ADC 530, and is switched in dependence upon the EN signal to output the digital U and V signals. As will be explained later herein, demultiplexer 540 produces both a digital U output signal and a digital V output signal during each clock cycle. One of these digital U and V output signals is a signal provided from ADC 530 during the current clock cycle, while the other of these digital U and V signals was provided from ADC 530 during a previous (e.g., immediately preceding) clock cycle. According to an exemplary embodiment, demultiplexer 540 holds previous U and V signal values such that it produces a current U output signal and a previous V output signal during one clock cycle, and then produces a previous U output signal and a current V output signal during the next clock cycle.

Filter 550 receives the digital U and V signals from demultiplexer 540, and performs a filtering (e.g., interpolating) operation thereon to thereby output time-aligned, filtered U and V signals in dependence upon the CLK signal. In particular, the filtered U and V signals produced by filter 550 are time-aligned relative to the corresponding input signals to multiplexer 520. In FIG. 5, filter 550 is shown as a single filtering device for operating upon both the U and V signal channels. In practicing the invention, however, filter 550 may be comprised of multiple filtering devices, such as a dedicated filter for each signal channel. Accordingly, filter 550 comprises at least one filtering device. According to an exemplary embodiment, filter 550 performs the filtering operations such that each U signal value is set equal to one half the U signal value received from demultiplexer 540 during the current clock cycle, plus one half the U signal value received from demultiplexer 540 during a previous (e.g., immediately preceding) clock cycle. Similarly, each V signal value is set equal to one half the V signal value received from demultiplexer 540 during the current clock cycle, plus one half the V signal value received from demultiplexer 540

during a previous (e.g., immediately preceding) clock cycle. Further details regarding this filtering operation will be provided later herein.

Subsampling device 560 receives the time-aligned, filtered U and V signals from filter 550, and performs a subsampling operation thereon to output subsampled U and V signals in a time-aligned manner in dependence upon the CLK signal and a subsample control ("SC") signal. The SC signal controls the frequency at which subsampling device 560 performs subsampling. For example, the SC signal may cause subsampling device 560 to perform subsampling upon a pair of filtered U and V signals every other clock cycle. The time-aligned U and V output signals from subsampling device 560 are then provided for further processing, such as color correction, tint correction, sample rate conversion, and/or other processing operation. Like filter 550, subsampling device 560 is shown in FIG. 5 as a single subsampling device for operating upon both the U and V signal channels. In practicing the invention, however, subsampling device 560 may be comprised of multiple subsampling devices, such as a dedicated subsampling device for each signal channel. Accordingly, subsampling device 560 comprises at least one subsampling device.

Referring to Table 4 below, further details regarding an exemplary operation of multiplexed ADC arrangement 500 will now be provided.

Clock Cycle	1	2	3	4	5
Analog U	45	46	47	48	49
Analog V	75	76	77	78	79
Mux Position	U	V	U	V	U
ADC Output	45	76	47	78	49
Demuxed U	45	45	47	47	49
Demuxed V	--	76	76	78	78
Filtered U	--	45	46	47	48
Filtered V	--	--	76	77	78

Table 4

As indicated in Table 4, analog U and V signals (i.e., Analog U and Analog V) are simultaneously input to multiplexer 520 during each clock cycle. The switching position of multiplexer 520 (i.e., Mux Position) changes from U to V in an alternating

manner from one clock cycle to another. In Table 4 for example, multiplexer 520 is switched to output an analog U signal having a value of 45 during clock cycle 1, and is switched to output an analog V signal having a value of 76 during clock cycle 2. Note also in Table 4 that certain U and V input signals to multiplexer 520 are lost. For example, during clock cycle 1, the V signal having a value of 75 is lost. Similarly, during clock cycle 2, the U signal having a value of 46 is lost. As will be indicated later herein, these lost signals are compensated for by the operation of filter 550.

ADC 530 receives the analog U and V output signals from multiplexer 520, and digitizes the received U and V signals in dependence upon the CLK signal. Since multiplexer 520 is switched such that every other U and V signal input to multiplexer 520 is lost, ADC 530 receives and digitizes only every other U and V signal input to multiplexer 520. For purposes of example and explanation, Table 4 illustrates ADC 530 as having a zero latency or delay between input and output. That is, Table 4 depicts ADC 530 as producing a digital U or V output signal (i.e., ADC Output) during the same clock cycle that it receives a corresponding analog U or V input signal from multiplexer 520. In practicing the invention, however, there may be some delay between the time at which ADC 530 receives an analog U or V input signal from multiplexer 520, and the time at which ADC 530 produces a corresponding digital U or V output signal. For example, such delay may be equal to one or more clock cycles.

Demultiplexer 540 receives the digitally converted U and V signals from ADC 530, and is switched in dependence upon the EN signal to simultaneously output digital U and V signals. Again, for purposes of example and explanation, Table 4 illustrates demultiplexer 540 as having a zero delay between input and output. Accordingly, Table 4 depicts demultiplexer 540 as producing a current U or V output signal (i.e., Demuxed U or Demuxed V) during the same clock cycle that it receives the current U or V signal from ADC 530. In practicing the invention, however, there may be some delay between the time at which demultiplexer 540 receives a U or V input signal from ADC 530, and the time at which demultiplexer 540 produces the U or V output signal. For example, such delay may be equal to one or more clock cycles.

As previously indicated herein, demultiplexer 540 produces both a digital U output signal and a digital V output signal during each clock cycle. In particular, demultiplexer 540 holds previous U and V signal values such that it produces a current U output signal and a previous V output signal during a given clock cycle, and then produces a previous U output signal and a current V output signal during the next clock cycle. For example, during clock cycle 3 in Table 4, demultiplexer 540 produces the current U output signal having a value of 47, and the V output signal of the immediately preceding clock cycle (i.e., clock cycle 2) having a value of 76. Then, during clock cycle 4, demultiplexer 540 produces the current V output signal having a value of 78, and the U output signal of the immediately preceding clock cycle (i.e., clock cycle 3) having a value of 47. In this manner, demultiplexer 540 produces both a digital U output signal and a digital V output signal during each clock cycle.

Filter 550 receives the digital U and V signals from demultiplexer 540, and performs a filtering operation thereon to thereby output time-aligned, filtered U and V signals. As previously indicated herein, filter 550 performs the filtering operation according to an exemplary embodiment such that each U signal value is set equal to one half the U signal value provided from demultiplexer 540 during the current clock cycle, plus one half the U signal value provided from demultiplexer 540 during a previous (e.g., immediately preceding) clock cycle. Similarly, each V signal value is set equal to one half the V signal value provided from demultiplexer 540 during the current clock cycle, plus one half the V signal value provided from demultiplexer 540 during a previous (e.g., immediately preceding) clock cycle. For example, during clock cycle 3 in Table 4, filter 550 outputs a filtered U signal (i.e., Filtered U) having a value of 46, and a filtered V signal (i.e., Filtered V) having a value of 76. The value of 46 for the filtered U signal is derived as follows:

$$\frac{1}{2}(47) + \frac{1}{2}(45) = 46$$

That is, for clock cycle 3 in Table 4, the filtered U signal is equal to one half the U signal value (i.e., 47) provided from demultiplexer 540 during the current clock cycle (i.e., clock cycle 3), plus one half the U signal value (i.e., 45) provided from demultiplexer 540 during the immediately preceding clock cycle (i.e., clock cycle 2). Similarly, the value of 76 for the filtered V signal is derived as follows:

$$\frac{1}{2}(76) + \frac{1}{2}(76) = 76$$

That is, for clock cycle 3 in Table 4, the filtered V signal is equal to one half the V signal value (i.e., 76) provided from demultiplexer 540 during the current clock cycle (i.e., clock cycle 3), plus one half the V signal value (i.e., 76) provided from demultiplexer 540 during the immediately preceding clock cycle (i.e., clock cycle 2). Of course, filter 550 may perform other types of filtering operations in accordance with the principles of the present invention. For example, filter 550 may generate filtered U and V signals by utilizing signal values from previous clock cycles other than the immediately preceding clock cycle.

Subsampling device 560 receives the time-aligned, filtered U and V signals from filter 550, and performs a subsampling operation thereon to generate subsampled U and V signals. Although not expressly shown in Table 4, subsampling device 560 outputs the subsampled U and V signals in a time-aligned manner during a subsequent clock cycle in dependence upon the CLK signal and the SC signal. As previously indicated herein, the subsampled U and V signals are provided for further processing, such as color correction, tint correction, sample rate conversion, and/or other processing operation.

Referring now to FIG. 6, a flowchart 600 summarizing exemplary steps for carrying out the present invention is shown. For purposes of example and explanation, the steps of FIG. 6 will be described with reference to multiplexed ADC arrangement 500 of FIG. 5.

In FIG. 6, process flow begins at step 601 where multiplexer 520 provides analog U and V input signals to ADC 530 in an alternating manner in dependence upon the EN signal. At step 602, ADC 530 converts the analog U and V input signals to a digital format, and outputs digital U and V signals to demultiplexer 540 in dependence upon the CLK signal, wherein each interval of the CLK signal defines a single clock cycle or time interval. At step 603, demultiplexer 540 in turn provides the digital U and V signals to filter 550 in dependence upon the EN signal. At step 604, filter 550 performs a filtering (e.g., interpolating) operation on the digital U and V signals provided from demultiplexer 540, and outputs filtered U and V signals to subsampling device 560 in a time-aligned manner in dependence upon the CLK signal. Then, at step 605, subsampling device 560 performs a subsampling operation on the filtered U and V signals provided from filter 550, and outputs subsampled U and V signals in a time-aligned manner. The time-aligned U and V

output signals from subsampling device 560 are then provided for further processing, such as color correction, tint correction, sample rate conversion, and/or other processing operation.

As described herein, the present invention advantageously eliminates analog delay means in a multiplexed ADC system that provides time-aligned output samples. Although the preferred embodiments have been described herein with reference to only two input signals (i.e., U and V), it will be intuitive to those skilled in the art that the principles of the present invention may be applied to systems having more than two input signals. Accordingly, the principles of the present invention may be applied to provide any number of signal channels with time-aligned output signals.

The present invention described herein is particularly applicable to various audio and/or video systems, either with or without display devices. Accordingly, the phase "audio and/or video system" or similar phases as used herein are intended to encompass various types of systems or apparatuses including, but not limited to, television sets or monitors that include a display device, and systems or apparatuses such as a set-top box, VCR, DVD player, video game box, PVR or other video system that may not include a display device. Moreover, the present invention may also be applicable to other systems, such as audio systems that may or may not have a video output.

While this invention has been described as having a preferred design, the present invention can be further modified within the spirit and scope of this disclosure. This application is therefore intended to cover any variations, uses, or adaptations of the invention using its general principles. Further, this application is intended to cover such departures from the present disclosure as come within known or customary practice in the art to which this invention pertains and which fall within the limits of the appended claims.

CLAIMS

1. A system (400), comprising:

an analog-to-digital converter (530) for converting first and second analog signals to first and second digital signals, respectively, and for outputting the first digital signal during a first time interval and outputting the second digital signal during a second time interval; and

a digital filter (550) for filtering the first and second digital signals to generate first and second filtered signals, respectively, and outputting the first and second filtered signals in a time-aligned manner during a third time interval.

2. The system (400) of claim 1, further comprising a multiplexer (520) for providing the first and second analog signals to the analog-to-digital converter (530).

3. The system (400) of claim 1, further comprising a demultiplexer (540) for receiving the first and second digital signals from the analog-to-digital converter (520), and providing the first and second digital signals to the digital filter (550).

4. The system (400) of claim 1, further comprising at least one subsampling device (560) for performing a subsampling operation upon the first and second filtered signals to generate first and second subsampled signals, respectively, and for outputting the first and second subsampled signals in a time-aligned manner during a fourth time interval.

5. The system (400) of claim 4, wherein the first, second, third and fourth time intervals each correspond to a single clock cycle.

6. The system (400) of claim 1, wherein:

the system (400) is a digital video system; and

the first and second digital signals are color difference signals.

7. An apparatus (500), comprising:

analog-to-digital conversion means (530) for converting first and second analog signals to first and second digital signals, respectively, and for outputting the first digital signal during a first time interval and outputting the second digital signal during a second time interval; and

digital filtering means (550) for filtering the first and second digital signals to generate first and second filtered signals, respectively, and for outputting the first and second filtered signals in a time-aligned manner during a third time interval.

8. The apparatus (500) of claim 7, further comprising multiplexing means (520) for providing the first and second analog signals to the analog-to-digital conversion means (530).

9. The apparatus (500) of claim 7, further comprising demultiplexing means (540) for receiving the first and second digital signals from the analog-to-digital conversion means (520), and providing the first and second digital signals to the filtering means (550).

10. The apparatus (500) of claim 7, further comprising subsampling means (560) for performing a subsampling operation upon the first and second filtered signals to generate first and second subsampled signals, respectively, and for outputting the first and second subsampled signals in a time-aligned manner during a fourth time interval.

11. The apparatus (500) of claim 10, wherein the first, second, third and fourth time intervals each correspond to a single clock cycle.

12. The apparatus (500) of claim 7, wherein:

the arrangement (500) is included in a digital video system (400); and

the first and second digital signals are color difference signals.

13. A method for processing signals in a system (400), comprising steps of:

converting first and second analog signals to first and second digital signals, respectively;

outputting the first digital signal during a first time interval;

outputting the second digital signal during a second time interval;

filtering the first and second digital signals to generate first and second filtered signals, respectively; and

outputting the first and second filtered signals in a time-aligned manner during a third time interval.

14. The method of claim 13, further comprising a step of multiplexing the first and second analog signals prior to the converting step.

15. The method of claim 13, further comprising a step of demultiplexing the first and second digital signals prior to the filtering step.

16. The method of claim 13, further comprising steps of:

performing a subsampling operation upon the first and second filtered signals to generate first and second subsampled signals, respectively; and

outputting the first and second subsampled signals in a time-aligned manner during a fourth time interval.

17. The method of claim 16, wherein the first, second, third and fourth time intervals each correspond to a single clock cycle.

18. The method of claim 13, wherein:

the system (400) comprises a digital video system; and

the first and second digital signals are color difference signals.

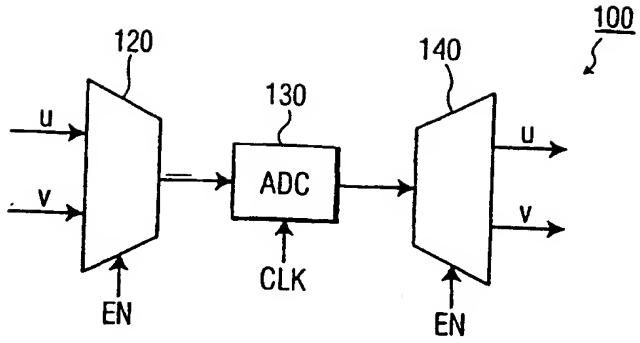

FIG. 1

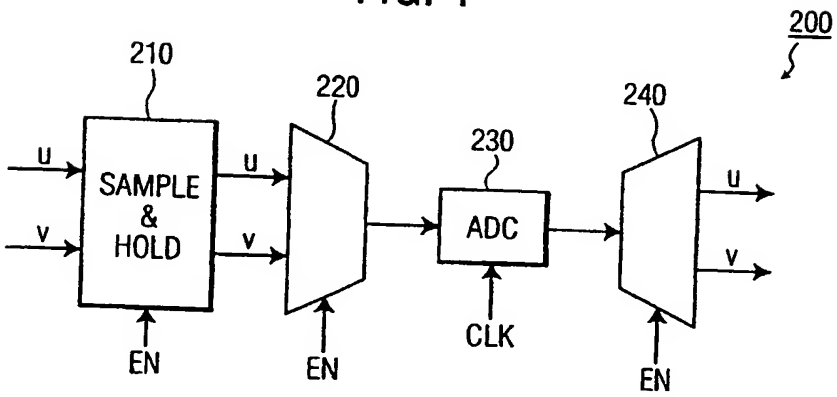

FIG. 2

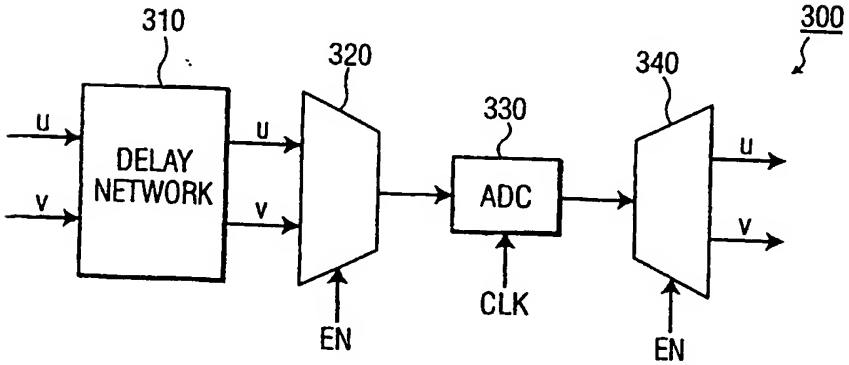

FIG. 3

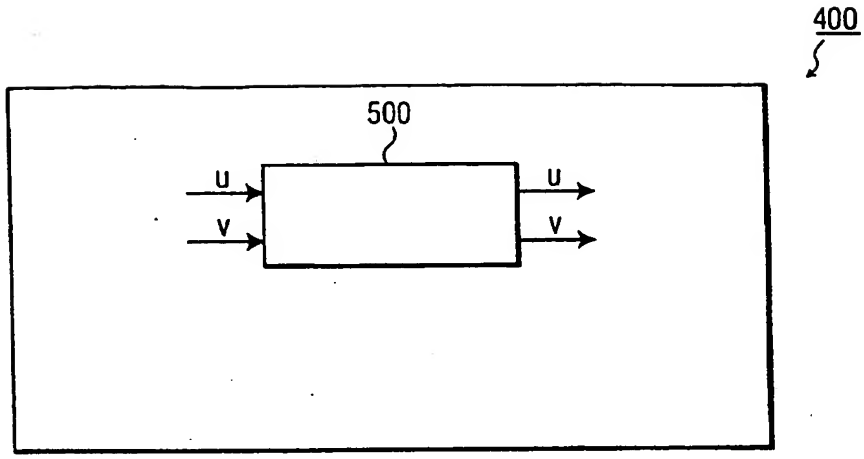
400
500
u
v
u
v

FIG. 4

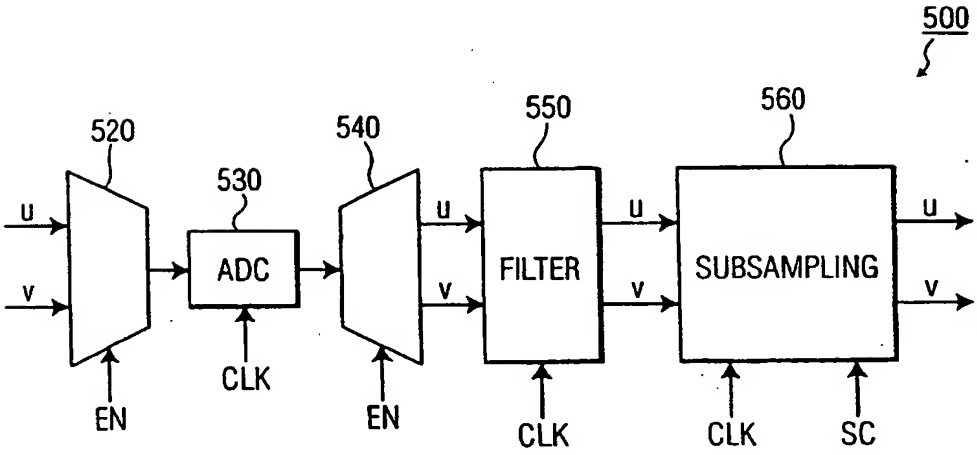
500
520
530
540
550
560
u
v
ADC
CLK
EN
u
v
EN
FILTER
CLK
u
v
SUBSAMPLING
CLK
SC
u
v

FIG. 5

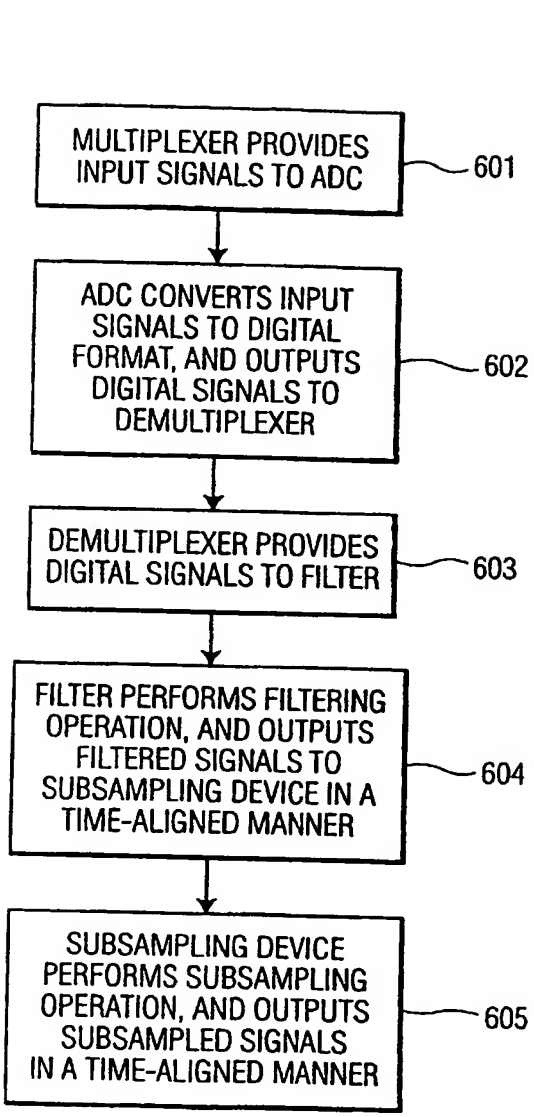
600
MULTIPLEXER PROVIDES INPUT SIGNALS TO ADC
601
ADC CONVERTS INPUT SIGNALS TO DIGITAL FORMAT, AND OUTPUTS DIGITAL SIGNALS TO DEMULTIPLEXER
602
DEMULTIPLEXER PROVIDES DIGITAL SIGNALS TO FILTER
603
FILTER PERFORMS FILTERING OPERATION, AND OUTPUTS FILTERED SIGNALS TO SUBSAMPLING DEVICE IN A TIME-ALIGNED MANNER
604
SUBSAMPLING DEVICE PERFORMS SUBSAMPLING OPERATION, AND OUTPUTS SUBSAMPLED SIGNALS IN A TIME-ALIGNED MANNER
605

FIG. 6

INTERNATIONAL SEARCH REPORT

Internati[illegible] Application No
PCT/US 02/39258

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04N5/45 H03M1/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04N H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US 5 459 528 A (PETTITT GREGORY S) 17 October 1995 (1995-10-17) abstract; figure 1 column 5, line 5-23 column 6, line 46-54	6,12,18
A	US 5 838 385 A (REDER JOHN R ET AL) 17 November 1998 (1998-11-17) column 4, line 46 -column 5, line 37	6,12,18

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 March 2003	19/03/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Gerdes, R

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INTERNATIONAL SEARCH REPORT

Internatic Application No
PCT/US 02/39258

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 013, no. 201 (E-757), 12 May 1989 (1989-05-12) & JP 01 022181 A (HITACHI LTD), 25 January 1989 (1989-01-25) abstract	6,12,18
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